IN THE SPECIFICATION:

Please amend paragraph number **[0008]** as follows:

[0008] In devices having one side of the substrate configured for a ball-grid-array (BGA) or similar array on a circuit board, the molding process is conducted so that the surface of the circuit board having the ball-grid-array connections ~~are~~ is formed on an outer surface of the package, such surface not being covered or encapsulated by the plastic material during the encapsulation process. When the substrate is sealably clamped on all sides of the cavity, plastic may reach the ball-grid-array side of the substrate only through the substrate, e.g., inadvertently through a hole or via. Of course, following removal from the cavity, any plastic encapsulant which may have reached and solidified on the ball-grid-array connection surface is removed.

Please amend paragraph number **[0009]** as follows:

[0009] The encapsulation process is typically performed before the "balls" of solder are placed on the pads of the grid ~~array,~~ array in order to prevent possible inadvertent disforming or loss of any solder balls during encapsulation.

Please amend paragraph number **[0010]** as follows:

[0010] As disclosed in the prior art, various integrated circuit devices are configured for one-side enclosure or ~~encapsulation,~~ encapsulation with an opposing bare or exposed side. United States Patent 5,598,034 to Wakefield discloses an electronic device having a lower bare surface of a metallic heat conductor to prevent overheating of the integrated circuit.

Please amend paragraph number **[0016]** as follows:

[0016] United States Patent 5,313,365 of Pennisi et al. discloses an electronic conductor-grid-array package including integrated circuits bonded to one side of a printed circuit board, and a grid array on the opposing side. Instead of using transfer molding techniques, the integrated circuits and associated wiring are encased in a glob-top encapsulant. Typically, ~~glob-~~

~~top~~ glob-top encapsulation is more time consuming, less reliable, and yields a product having a less pleasing appearance than conventional transfer molding methods.

Please amend paragraph number **[0017]** as follows:

[0017] The invention comprises an improved method and apparatus for encapsulating or enclosing electronic devices mounted on the first side of a substrate such as a circuit board or wiring board. The invention may be particularly applied to one-side encapsulation or enclosing of electronic devices which includes a substrate such as a circuit board configured to have a ball-grid-array (BGA), ~~pin-grid-array~~ pin-grid-array (PGA), land-grid-array (LGA) or similar set of multiple electrical terminals on its opposite side. The array of terminals of such a substrate is typically configured to be bonded to terminals of another apparatus following encapsulation of the electronic devices including IC chip(s), leads, wiring and/or other components on its first side with plastic.

Please amend paragraph number **[0037]** as follows:

[0037] A method for rapid one-side encasing of array packages and an apparatus for performing such packaging are described. The several aspects of the invention are particularly applicable to substrate-mounted arrays of ball grids, pin grids and land grids with various ~~encapsulable~~ encapsulatable devices mounted on the opposite side of the substrate. In addition, devices having exposed heat sinks or heat radiators on the opposite side of an otherwise impermeable substrate may be rapidly one-side encapsulated by the method and apparatus of the invention. The method and apparatus are applicable to any device including a generally planar substrate, wherein one side of the substrate is to be non-encapsulated in the final packaged form.

Please amend paragraph number **[0042]** as follows:

[0042] In accordance with the invention, two electronic devices 50A and 50B are shown within the mold cavity 16, in a back-to-back orientation, the second sides 56A and 56B of substrates 18A and 18B, respectively, in abutment. Upper electronic device 50A comprises a

planar substrate 18A having a first side 48A upon which a semiconductor die 52A is attached and electrically connected thereto by wires 54A. Likewise, lower electronic device 50B is shown as comprising a planar substrate 18B having a first side 48B upon which a semiconductor die 52B is attached and electrically connected via wires 54B or some other suitable method. The first and second electronic devices 50A, 50B may each have an array of conductive terminals, e.g. pads, not visible, on its substrate second side 56A or 56B, respectively, each array of terminals connected by conductors (not shown) passing through the respective substrate 18A or 18B to the wires 54A, 54B of the device.

Please amend paragraph number **[0043]** as follows:

[0043] It is understood that the two electronic devices 50A, 50B may be substantially identical, or may differ, for example, in the particular numbers and types of components attached to the substrate, in substrate composition and thickness, etc. The specifications of the two electronic devices 50A and 50B may differ with respect to the encapsulant, and the mold plates 12, 14 and methods of this invention provide for simultaneous one-side encapsulation of different devices with different materials. Materials typically used for such encapsulation include epoxy resins, organosilicon polymers, polyimide, etc.

Please amend paragraph number **[0044]** as follows:

[0044] The upper mold plate 12 generally has a flat upper surface 42, and the lower mold plate 14 has a flat lower surface 44. Following placement of the electronic devices 50A, 50B back-to-back between the mold plates 12, 14, compressive forces 46 are exerted upon surfaces 42, 44 to clamp the mold plates 12, 14 against the pair of substrates 18A, 18B, and the encapsulation process may proceed without leakage. The array of terminals is configured to be positioned outside of the area under high compression to avoid damage to the terminals. Thus, the area under compression is "circumferential" about each cavity, where "circumferential" refers to the excluded area rather than any circularity. The cavities are usually rectangular in shape rather than round.

Please amend paragraph number **[0047]** as follows:

[0047] A buffer member 60 is illustrated in FIG. 4 as a flat or planar body typically with parallel surfaces 72A, 72B, and having thickness 68. Typically, the buffer member 60 will be continuous and generally coextensive with each strip of ~~substrate~~ substrates 18A, 18B. The buffer member 60 may alternatively be formed of multiple portions more readily fitted to the arrays of balls, pins, pads, etc.

Please amend paragraph number **[0050]** as follows:

[0050] Second, the buffer member 60 absorbs some of the compressive forces 46 exerted during the encapsulation, protecting the array of terminals from breakage or distortion.

Please amend paragraph number **[0052]** as follows:

[0052] Fourth, the buffer member 60 enhances the ease of separating the two ~~array~~ electronic devices 50A, 50B without damage, following encapsulation.

Please amend paragraph number **[0055]** as follows:

[0055] In FIG. 5, the molding plates of FIG. 1 are shown in a method for one-side encapsulation of a pair of typical electronic devices 50A and 50B, each comprising ~~components 52A (or 52B)~~ dice and wires 52A, 54A (or 52B, 54B) mounted on a substrate 18A (or 18B) such as a circuit board with a ball-grid-array of solder balls 62A, 62B, respectively. The electronic devices 50A, 50B are placed back-to-back in the mold cavity 16, with an intervening buffer member 60. The substrates and buffer member 60 form a "laminar" arrangement, though they are not attached to each other. As depicted in FIGS. 5 and 6, the buffer member 60 includes cut-out 64 into which the arrays of solder balls 62A and 62B are positioned. The thickness 68 of the buffer member 60 in a compressed condition enables the solder balls 62A, 62B from both substrates 18A, 18B to fit within the cut-out 64 without touching, so that deformation or damage to the solder balls is avoided. For typical ball-grid-arrays (BGA), the thickness 68 of the buffer

member 60 will be sufficient to accommodate both sets of solder balls 62A, 62B. Where used for pin-grid-arrays (PGA), the required thickness will vary depending upon pin length.

Please amend paragraph number **[0059]** as follows:

[0059] FIGS. 7 and 8 illustrate a further embodiment of the invention. The buffer member 60 is perforated with groupings 70 of cut-outs 66 to accommodate array pads, balls, pins, etc. which protrude from the bare substrate second sides 56A, 56B and which otherwise would impinge on both parallel surfaces 72A, 72B of the buffer member. The cut-outs 66 are aligned with the conductors and are of such a size to accommodate the usual variability in positioning of the substrates 18A, 18B on the buffer member 60. The cut-outs 66 in the buffer member 60 may be formed by any method capable of forming small holes, including laser cutting or "drilling," and extend from the upper parallel surface 72A to the lower parallel surface 72B.

Please amend paragraph number **[0067]** as follows:

[0067] In accordance with the invention, two electronic devices 50A and 50B are shown within the cavity 116, in a back-to-back orientation, the substrate second sides 56A and 56B, respectively, in abutment. Upper electronic device 50A comprises a planar substrate 18A having a first side 48A upon which a semiconductor die component 52A is attached and electrically connected thereto by wires 54A or some other suitable connection. Likewise, lower electronic device 50B is shown as comprising a planar substrate 18B having a first side 48B upon which a semiconductor die component 52B is attached and electrically connected via wires 54B. The first and second electronic devices 50A, 50B may each have an array of conductive terminals, e.g. pads, not visible, on substrate second side 56A or 56B, respectively, each array of terminals connected by conductors (not shown) passing through the respective substrate 18A or 18B to the wires 54A, 54B of the device.

Please amend paragraph number **[0068]** as follows:

[0068] Contained within upper cavity portion 116A of upper plate 112 is a cover 130 being held therein through the use of a vacuum supplied through aperture 126 after being placed therein in any suitable manner. Similarly, contained within lower cavity portion 116B of lower plate 114 is a cover 130 being held therein through the use of a vacuum supplied through aperture 126 after being placed therein in any suitable manner. The covers 130 may be of any type of suitable material in any suitable shape for application to the substrate 18A or 18B to encase the semiconductor die ~~component~~ components 52A and 52B, respectively.

Please amend paragraph number **[0070]** as follows:

[0070] The upper plate 112 generally has a flat upper surface 142, and the lower plate 114 has a flat lower surface 144. Following placement of the electronic devices 50A, 50B back-to-back between the plates 112, 114, compressive forces 46 are exerted upon surfaces 142, 144 to clamp the plates 112, 114 against the pair of substrates 18A, 18B and the process proceeds to attach, such as by using adhesive bonding, the covers 130 to the ~~substrate~~ substrates 18A, 18B. The lower edge of each cover 130 may be coated with a suitable adhesive to attach the cover 130 to the ~~substrate~~ substrates 18A, 18B. The wire bonds to the circuits of the ~~substrate~~ substrates 18A, 18B are placed to be located outside the area of compression of the edge of the cover 130 on the ~~substrate~~ substrates 18A, 18B. As stated, the cover 130 may be of any shape desired to enclose and isolate a desired area on the ~~substrate~~ substrates 18A, 18B.

Please amend paragraph number **[0071]** as follows:

[0071] Referring to FIG. 10, another embodiment of the present invention is shown such as illustrated in FIG. 9, except that each cover 130 has the lower edge thereof secured in a recess 18C or 18D formed in ~~substrate~~ substrates 18A, 18B, respectively. The lower edge of cover 130 may be secured in the ~~recess~~ recesses 18C, 18D of ~~substrate~~ substrates 18A, 18B, respectively, by means of a suitable adhesive or any other suitable, well-known attachment.

Please amend paragraph number **[0072]** as follows:

[0072] Referring to FIG. 11, another embodiment of the present invention is shown wherein the plates of FIG. 9 are used for one-side encapsulation of a pair of typical electronic devices 50A and 50B, each comprising ~~components 52A (or 52B)~~ dice and wires 52A, 54A (or 52B, 54B) mounted on a substrate 18A (or 18B) such as a circuit board with a ball-grid-array of solder balls 62A, 62B, respectively. The electronic devices 50A, 50B are placed back-to-back in the mold cavity 116, with an intervening buffer member 60. The substrates and buffer member 60 form a "laminar" arrangement, though they are not attached to each other. As depicted in FIGS. 11 and 5, the buffer member 60 includes a cut-out 64 into which the arrays of solder balls 62A and 62B are positioned. The thickness 68 of the buffer member 60 in a compressed condition enables the solder balls 62A, 62B from both substrates 18A, 18B to fit within the cut-outs 64, 66 (shown in FIG. 12) without touching, so that deformation or damage to the solder balls is avoided. The cover 130 is attached to ~~substrate~~ substrates 18A, 18B by any suitable arrangement, such as adhesive bonding, etc.

Please amend paragraph number **[0073]** as follows:

[0073] Referring to FIG. 12, another embodiment of the invention is shown with the outer edge of cover 130 being retained in ~~a recess~~ recesses 18C, 18D of the ~~substrate~~ substrates 18A, 18B respectively. The cover 130 may be secured in the ~~recess~~ recesses 18C, 18D of ~~substrate~~ substrates 18A, 18B by any suitable arrangement, such as adhesive bonding, etc.